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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2677	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,693	KOYAMA ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-27,80-87 and 105-123* is/are pending in the application.

4a) Of the above claim(s) *1-10,36-45,54-61,71-79 and 88-104* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-27,80-87,105-123* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 19, 25, 80, 105-106, 112, 115-116 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinya (US Patent No. 5,170,158).

As to claim 19, Shinya teaches an image display device (See Col, 1, Lines 6-10), comprising:

a pixel array portion including a plurality of signal lines (See Fig. 1, item 2), a plurality of scan lines (See Fig. 1, item 3), a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other (See Fig. 1, item 4), and plurality of switching elements for driving the plurality of pixel electrodes (See Fig. 1, item 5, Col. 1, Lines 21-30);

a signal line driver circuit for driving the plurality of signal lines (See Fig. 1, item 6, Col. 1, Lines 31-32); and

a scan line driver circuit for driving the plurality of scan lines (See Fig. 1, item 7, Col. 1, Lines 32-39),

wherein signal line driver includes an integral multiple of 8 shift registers (in reference inside of each item 13 are 8 shift registers (DFFs in Figure 1 of the application) connected in series, with 8 outputs to DAC) to which m-bit

(m is natural number) (in reference 8) digital picture signals are inputted (See first example and Fig. 2, item 13, Col. 4, Lines 1-12),

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (Fig. 2, item 15, Col. 4, Lines 1-7), and a plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 2, items P1-Pn, Col. 4, Lines 16-23), and

wherein an operation in which the digital picture signals are inputted to the respective shift registers (See Fig. 2, items 13-14, S1-S4, Col. 4, Lines 16-20) the inputted digital picture signals are sequentially shifted in the respective shift registers and is repeated n (N is an integer not less than 2) times in a time corresponding to one horizontal scan period (see Figs. 2-4, items 13-17, Col. 4, lines 28-62).

The first example of Shinya does not disclose a plurality of storage circuits for storing output signals of the shift registers by a latch signal.

The third example of Shinya teaches a plurality of storage circuits for storing output signals of the shift registers by a latch signal (See Fig. 10, item 21, Col. 7, Lines 3-18).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by different examples of Shinya because of small driver circuit size requirements (See Col. 1, Lines 16-18 in the Shinya reference).

As to claim 80, Shinya teaches a signal driver circuit of an image display device (See Col, 1, Lines 6-10) for driving the plurality of signal lines (See Fig. 1, item 6, Col. 1, Lines 31-32), the signal line driver circuit comprising:

an integral multiple of 8 shift registers (in reference inside of each item 13 are 8 shift registers (DFFs in Figure 1 of the application) connected in series, with 8 outputs to DAC) to which m-bit (m is natural number) (in reference 8) digital picture signals are inputted (See first example and Fig. 2, item 13, Col. 4, Lines 1-12),

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (Fig. 2, item 15, Col. 4, Lines 1-7), and

a plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (see Fig. 2, items P1-Pn, Col. 4, Lines 16-23),

wherein an operation in which the digital picture signals are inputted to the respective shift registers (See Fig. 2, items 13-14, S1-S4, Col. 4, Lines 16-20) the inputted digital picture signals are sequentially shifted in the respective shift registers and is repeated n (N is an integer not less than 2) times in a time corresponding to one horizontal scan period (see Figs. 2-4, items 13-17, Col. 4, lines 28-62).

The first example of Shinya does not disclose a plurality of storage circuits for storing output signals of the shift registers by a latch signal.

The third example of Shinya teaches a plurality of storage circuits for storing output signals of the shift registers by a latch signal (See Fig. 10, item 21, Col. 7, Lines 3-18).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by different examples of Shinya because of small driver circuit size requirements (See Col. 1, Lines 16-18 in the Shinya reference).

As to claim 105, Shinya teaches an image display device (See Col, 1, Lines 6-10), comprising:

a pixel array portion including a k of signal lines (See Fig. 1, item 2), a plurality of scan lines (See Fig. 1, item 3), a plurality of pixel electrodes provided at respective regions where the respective signal lines and the respective scan lines intersect with each other (See Fig. 1, item 4), and plurality of switching elements for driving the plurality of pixel electrodes (See Fig. 1, item 5, Col. 1, Lines 21-30);

a signal line driver circuit for driving the k of signal lines (See Fig. 1, item 6, Col. 1, Lines 31-32); and

a scan line driver circuit for driving the plurality of scan lines (See Fig. 1, item 7, Col. 1, Lines 32-39),

wherein signal line driver includes an integral multiple of 8 shift registers (in reference inside of each item 13 are 8 shift registers (DFFs in Figure 1 of the application) connected in series, with 8 outputs to DAC) to which m-bit

(m is natural number) (in reference 8) digital picture signals are inputted (See first example and Fig. 2, item 13, Col. 4, Lines 1-12),

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (Fig. 2, item 15, Col. 4, Lines 1-7), and a k/n (in reference N/M) of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 2, items P1-Pn, Col. 4, Lines 16-23

The first example of Shinya does not disclose a m x k/n of storage circuits for storing output signals of the shift registers by a latch signal.

The third example of Shinya teaches a plurality of storage circuits (equal to the number of the DAC) for storing output signals of the shift registers by a latch signal (See Fig. 10, item 21, Col. 7, Lines 3-18).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by different examples of Shinya because of small driver circuit size requirements (See Col. 1, Lines 16-18 in the Shinya reference).

As to claim 115, Shinya teaches a signal driver circuit of an image display device (See Col, 1, Lines 6-10) for driving the k of signal lines (See Fig. 1, item 6, Col. 1, Lines 31-32, the signal line driver circuit comprising:

shift registers to which m-bit (m is a natural number) (in reference 8) digital picture signals are inputted, the number of the shift registers being an integral multiple of m (in reference inside of each item 13 are 8 shift registers

(DFFs in Figure 1 of the application) connected in series, with 8 outputs to DAC) (See first example and Fig. 2, item 13, Col. 4, Lines 1-12),

a plurality of D/A converter circuits for converting output signals of the storage circuits into analog signals (Fig. 2, item 15, Col. 4, Lines 1-7), and

a k/n (in reference N/M) of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 2, items P1-Pn, Col. 4, Lines 16-23)

The first example of Shinya does not disclose a m x k/n of storage circuits for storing output signals of the shift registers by a latch signal.

The third example of Shinya teaches a plurality of storage circuits (equal to the number of the DAC) for storing output signals of the shift registers by a latch signal (See Fig. 10, item 21, Col. 7, Lines 3-18).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement different elements of the source driver as shown by different examples of Shinya because of small driver circuit size requirements (See Col. 1, Lines 16-18 in the Shinya reference).

As to claim 25, 112, Shinya teaches a display is carried out using a liquid crystal material (see Col. 1, Lines 12-19).

As to claim 106, 116, Shinya teaches the number of converter circuits is 4 (k/8 X 2) (See Fig. 2, item 15, Col. 5, Lines 38-48).

2. Claims 20-24, 81-85, 107-111 and 117-121 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinya as applied to claims 19, 80,

105 and 115 above, and further in view of Luder et al. (US Patent No. 5,642, 117).

As to claim 20, 81, 107 and 117, Shinya does not disclose a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch.

Luder et al. teaches a ramp type D/A converter with bit comparison pulse width converter circuit and analog switch (See Fig. 1, items a0-a3, b0-b3, 10-13, Sr, C, in description See from Col. 5, to Col. 6, Line 8).

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bit comparison pulse width converter circuit and analog switch as shown by Luder et al. in Shinya system in order to optimize digital/analog conversion so that as little circuitry expense as possible is required (See Col. 2, Lines 16-19 in the Luder et al. reference).

As to claim 21-24, 82-85, 108-111 and 118-121, Shinya does not disclose the storage circuit is a latch circuit with analog switch, holding capacitance with clocked inverter and a plurality of inverters.

Luder et al. teaches the storage circuit is a latch circuit with analog switch, holding capacitance with clocked inverter and a plurality of inverters (See Figs. 14A-14B, items Q1-Q2, nQ1-Nq2, 400, 420, 430, Col. 9, Lines 51-67 and Col. 10, Lines 1-21).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Luder et al. into Shinya system in order to reduce cost (See Col. 2, Lines 16-19 in the Luder et al. reference).

3. Claims 26, 113 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinya as applied to claims 19, 105 above, and further in view of Friend et al. (US Patent No. 5,247, 190).

Shinya does not disclose a display is carried out using an electroluminescence material.

Friend et al. teaches a display is carried out using an electroluminescence material (See Fig. 3, items 3-5, Col. 8, Lines 5-20).

It would have been obvious to one of ordinary skill in the art at the time of invention to use materials as shown by Friend et al. in Shinya system in order to increase the range of applications.

4. Claims 27, 114 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinya as aforementioned in claims 19, 105 in view of Matsueda et al (US Patent No. 6,384,806 B1).

Shinya does not teach a portable telephone, which uses the image display device.

Matsueda et al. shows a portable telephone, which uses the image display device (See Fig. 19-22, in description See Col. 23, Lines 10-15).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the Shinya apparatus in the portable telephone as shown by Matsueda et al. in order to increase the range of applications.

5. Claims 86-87, 122-123 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinya as aforementioned in claims 81, 115 in view of Lewis (US Patent No. 5,589,847).

Shinya does not teach the driver circuit is formed of a poly silicon thin film transistor or of a single crystal transistor.

Lewis teaches the driver circuit is formed of a poly silicon thin film transistor or of a single crystal transistor (See Abstract).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Lewis into the Shinya system in order to increase the mobility of transistors.

Response to Arguments

6. Applicant's arguments filed on 10.25.05 have been fully considered but they are not persuasive:

On page 17, 6 paragraph of Remarks, Applicant's stated that Shinya discloses in Fig. 2 one-half of n-bit registers and Shinya does not teach or suggest an integral multiple of n shift registers. However, each of 4 registers in the reference has 8 shift registers (stages or DFFs) inside of the item 13, which is equivalent to the DFFs in Figure 1 of the Application. Only difference, that in Figure 1 of Application all 3 DFFs are connected in parallel, but in the reference in Figure 2 they are connected in series. Notice that in the reference Figure 2, there are 8 outputs from the shift registers to the DACs, and in Application Figure

1, only 3, correspondent to the number of DFF or shifting stages (See Col. 4, Lines 13-15 in the Shinya reference).

On page 17, the same paragraph of Remarks, Applicant's stated that Shinya does not disclose any circuit which correspondent to ' a plurality of signal line selection circuits". However, even in Abstract Shinya teaches that the D/A converters are repeatedly used to sequentially convert portions of the input digital image signal correspondent to one horizontal scanning line, and also Shinya teaches plurality of signal line selecting circuits for transmitting output signals of the D/A converter circuits to the corresponding signal lines (See Fig. 2, items P1-Pn, Col. 4, Lines 16-23). Connection to signal lines done through S/H and amplifiers (See Fig. 2, items 15-18).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AMR A. AWAD
PRIMARY EXAMINER

LS
12.22.05